SytHIL: A System Level Hardware-in-the-Loop Framework for FPGA, SystemC and QEMU-based Virtual Platforms

A RISC-V example using AWS cloud servers

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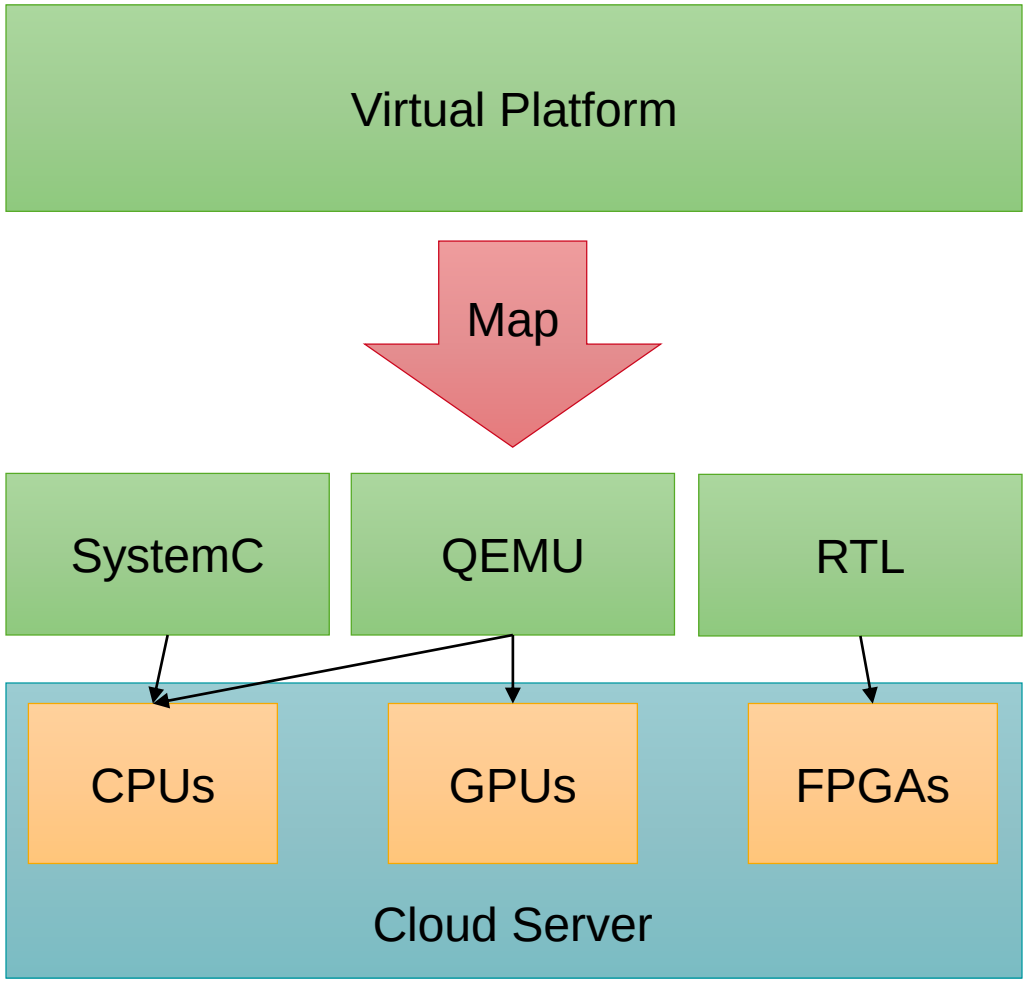
Motivation

Problem
- HW/SW systems increasingly complex
- RTL verification is hard to scale
  - Simulation is slow
  - Emulation is expensive
  - Prototyping is expensive

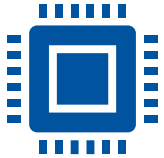
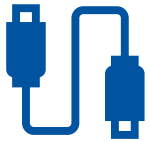
Approach
- Hybrid Prototyping: Simulation + RTL on FPGA
  - Parts on FPGA, simulation provides test environment
  - Speed of VP + accuracy of FPGA

Innovation
- FPGAs available in the cloud
  - Low entrance barrier, pay as you go
  - Scalable

➢ Integrate cloud FPGAs and SystemC TLM-2.0 VPs



Agenda

- Hybrid Prototyping 
- Cloud FPGAs 
- Simulation Setup 
- DMI and AWS FPGAs 
- Demo 
- Conclusion 

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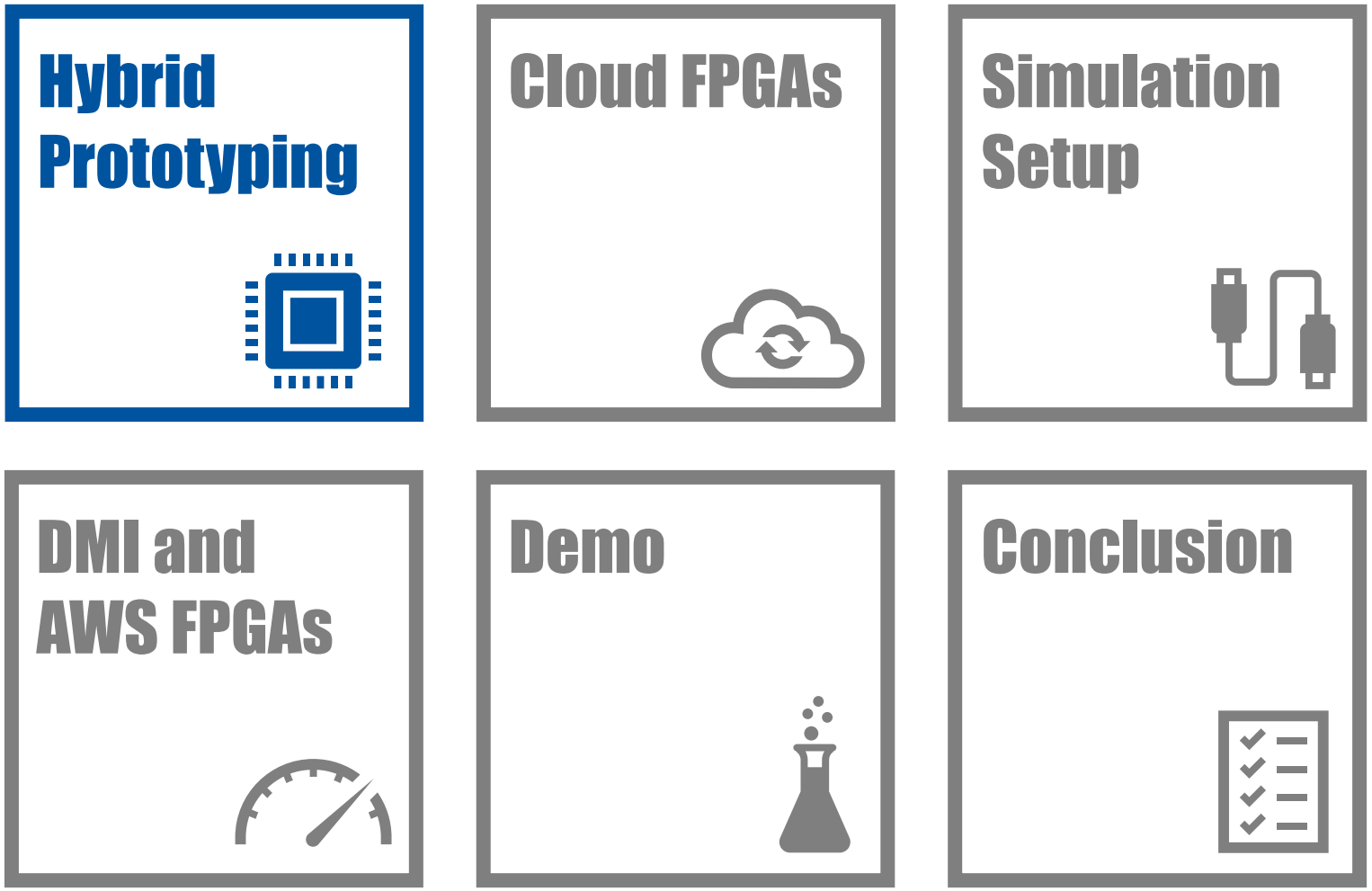
Hybrid Prototyping
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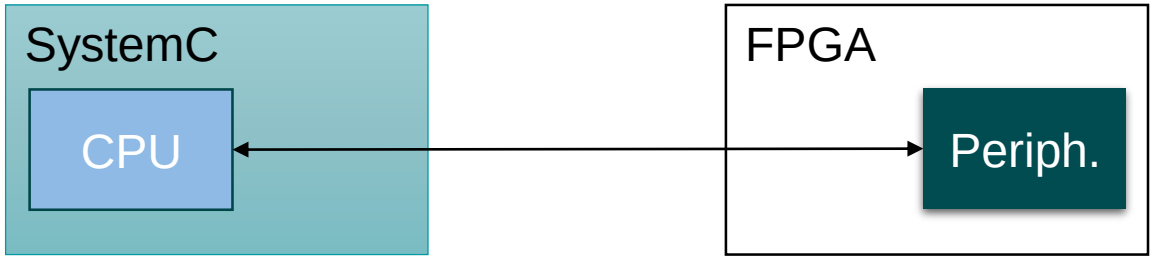
Hybrid Prototyping

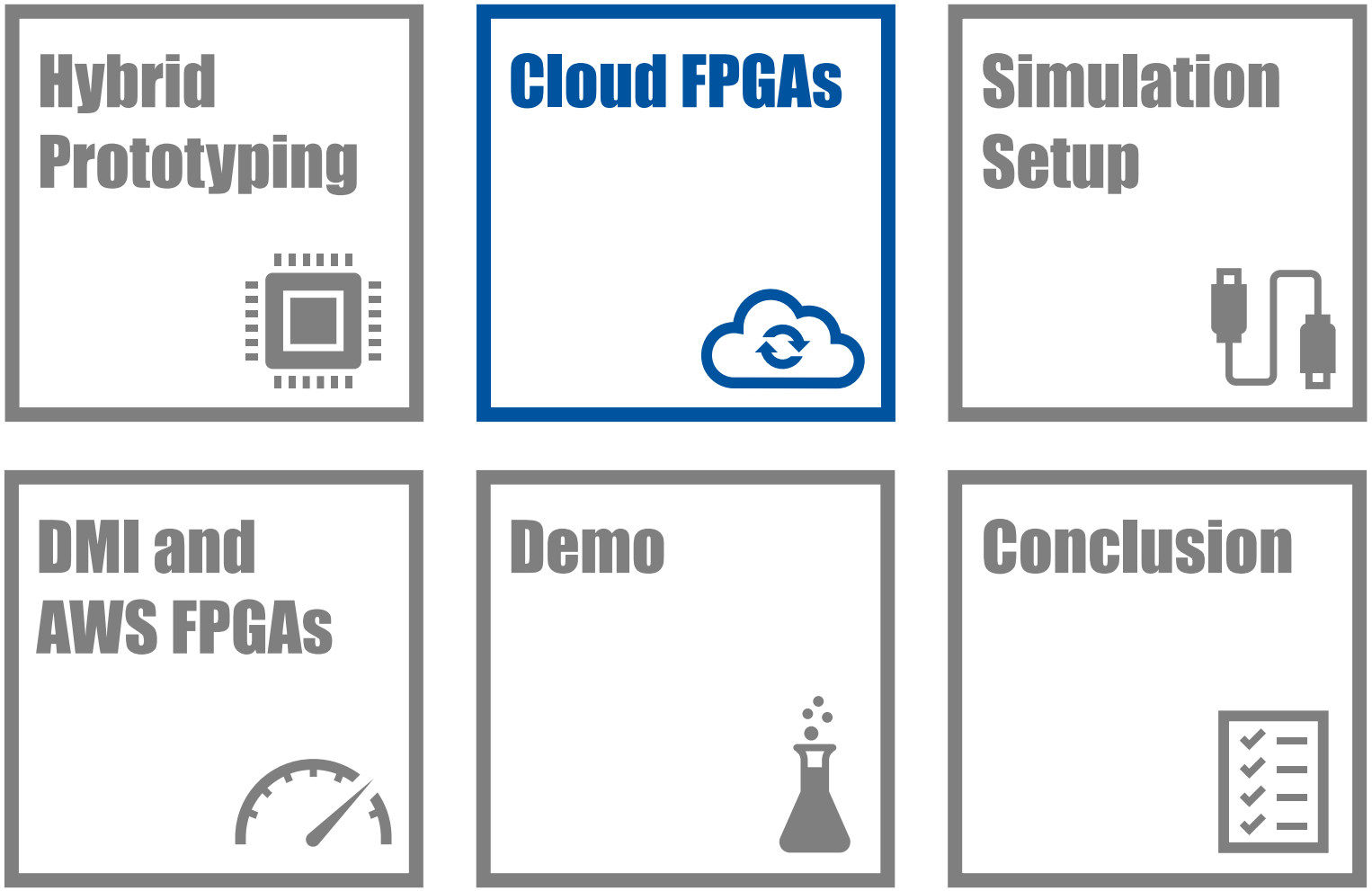
- Design hardware and software simultaneously
  - Write Linux driver before device is available
- Transition from virtual to FPGA prototype
- Write testbench in SystemC



- Software development on RTL
- Functional hardware verification
- Peripheral integration

- Commericial Solutions:
  - Synopsys HAPS
  - Siemens Veloce Primo
  - Cadence Protium

Agenda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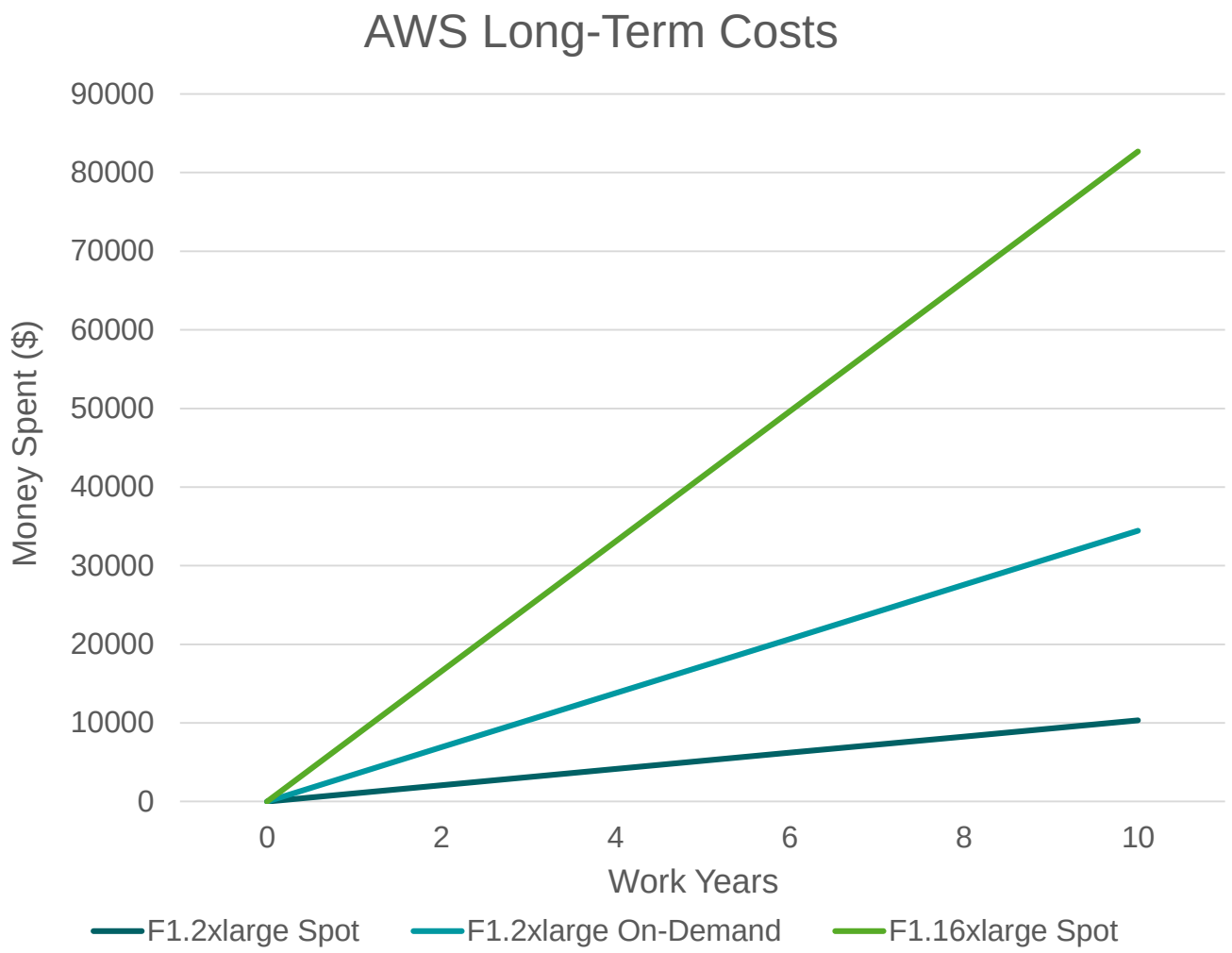
The Cloud

- Scalability
  - Enables testing
  - Enables design exploration
- Hardware for multiple people
- Reproducable setup
- Hardware gets upgraded
- Reduced upfront cost

Specs	F1.2xlarge	F1.16xlarge
FPGAs	1	8
vCPUs	8	64
On-Demand	1.65 $/h	13.3 $/h
Spot Instance	0.495 $/h	3.96 $/h

- 8-hour workdays, 261 workdays per year
- Sums up to 2088 h/year
- 10.000$ with F1.2xlarge spot instance:
  - 9.6 work years



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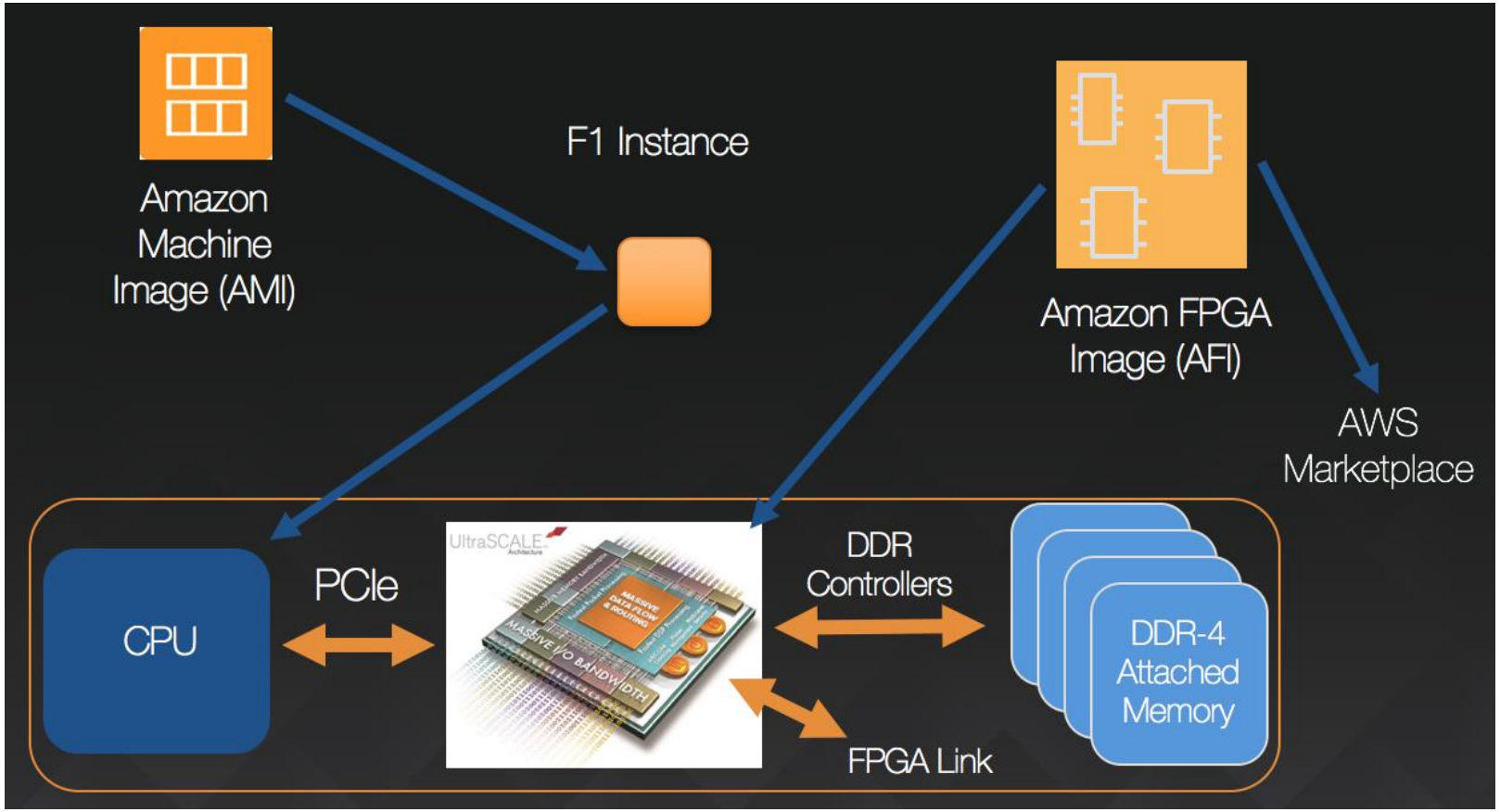
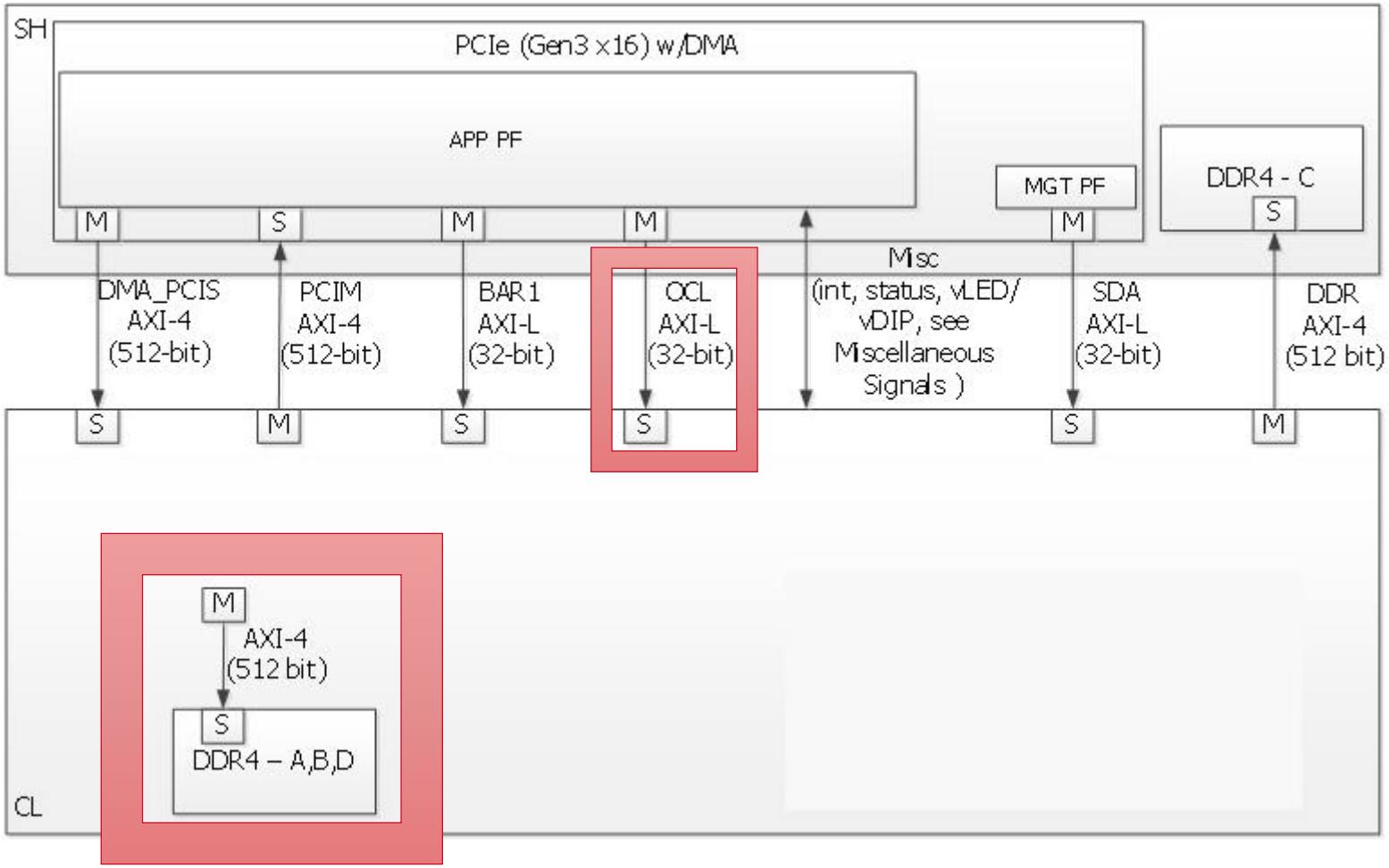
AWS Infrastructure



AWS Shell



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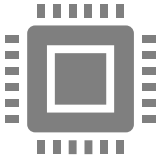
- Hybrid Prototyping 
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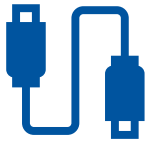
- **Simulation Setup** 
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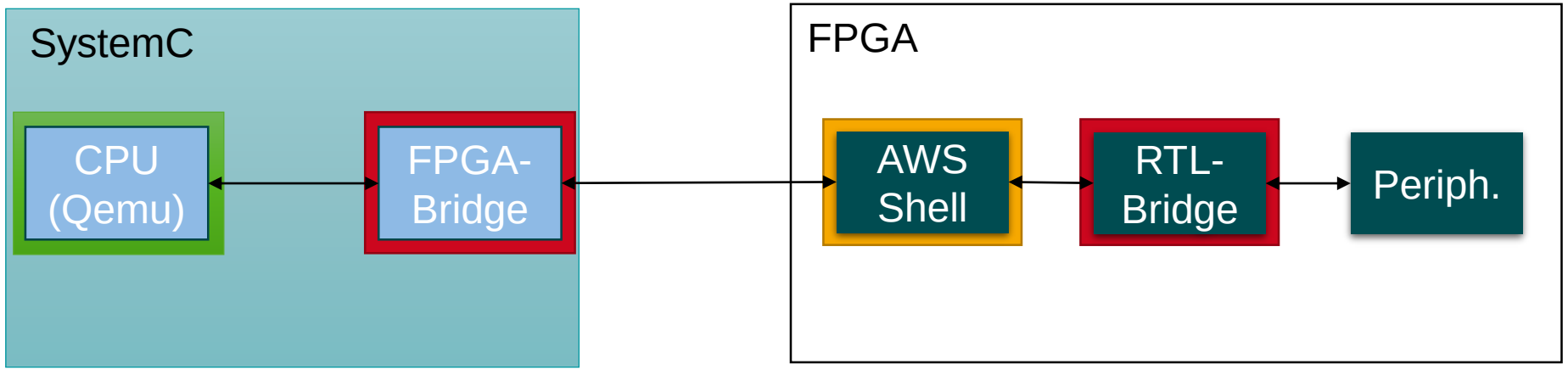
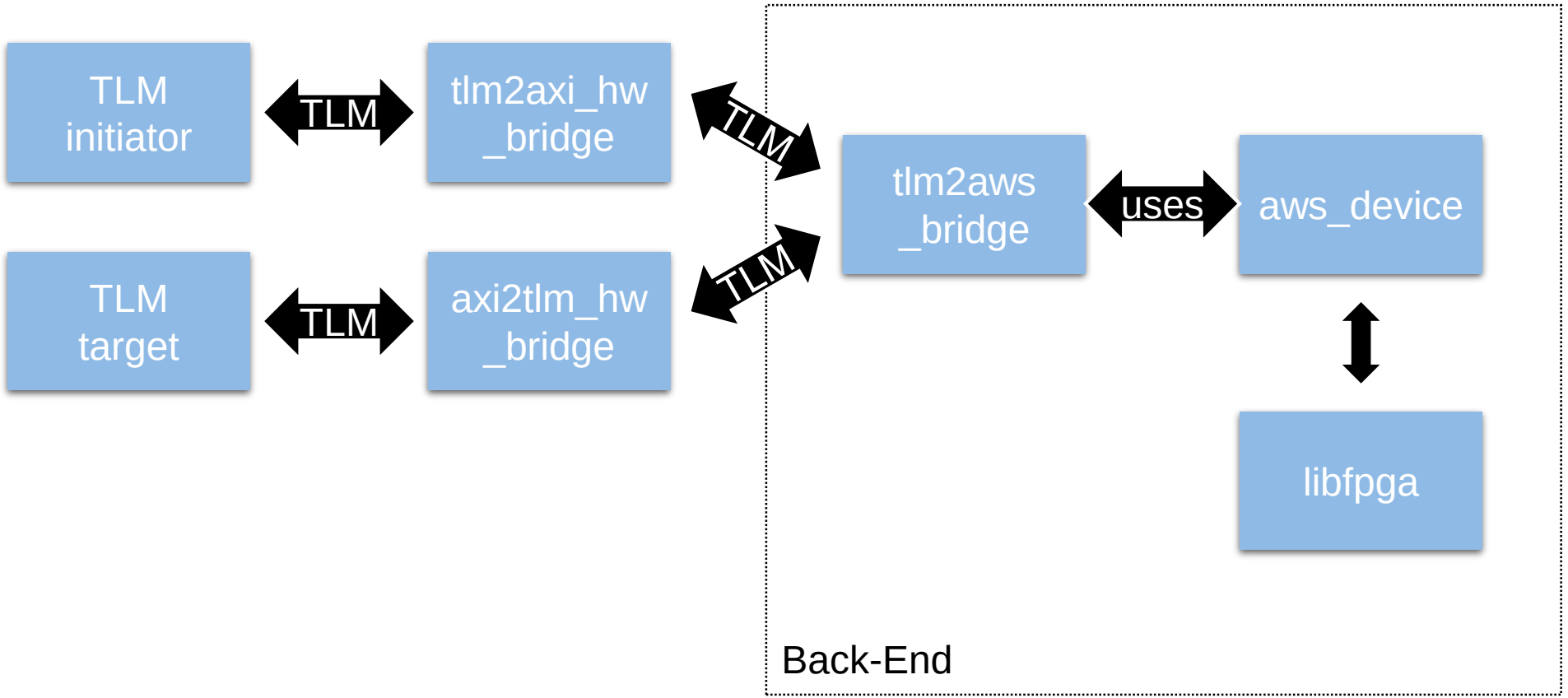
Dataflow Mechanism

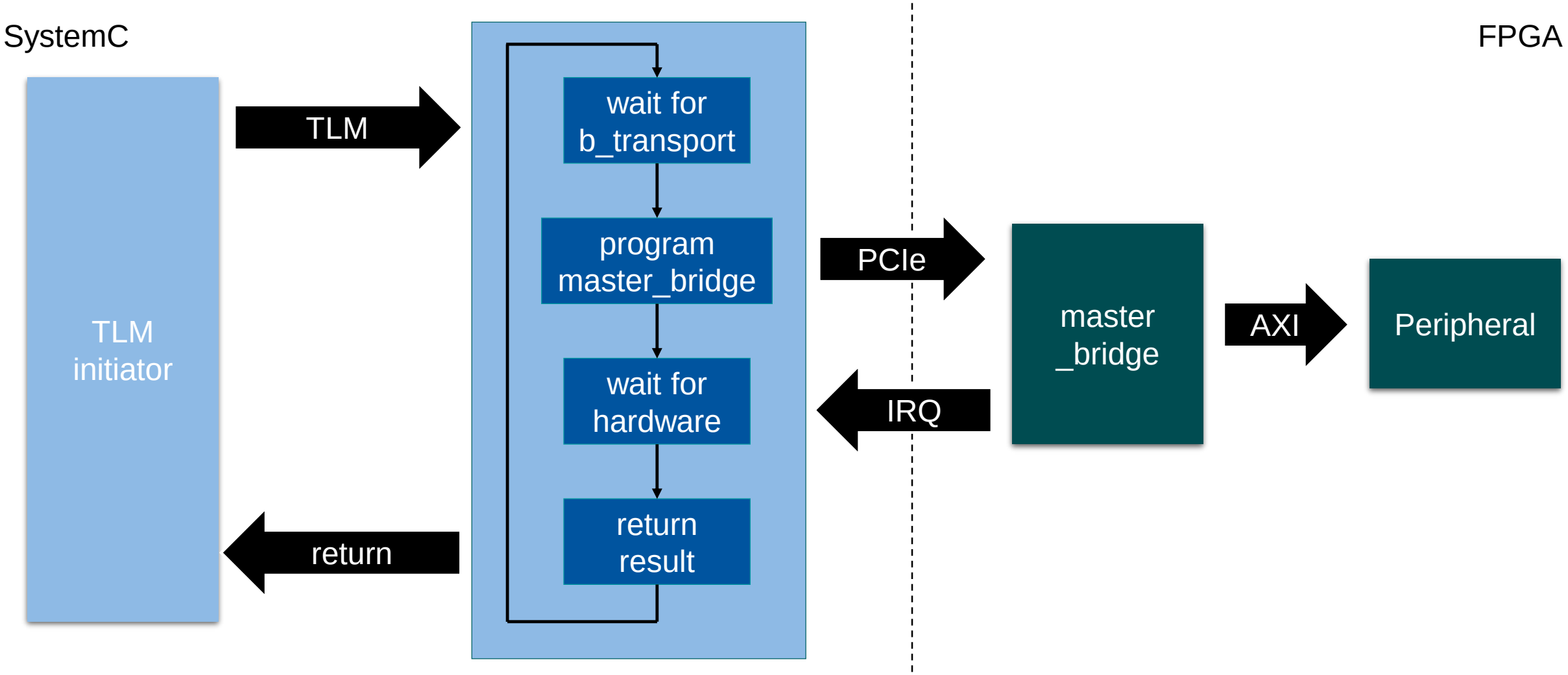
- Xilinx‘s library contains modules that allow co-simulation with SystemC and RTL
- GreenSocs‘s Qbox allows co-simulation of Qemu and SystemC



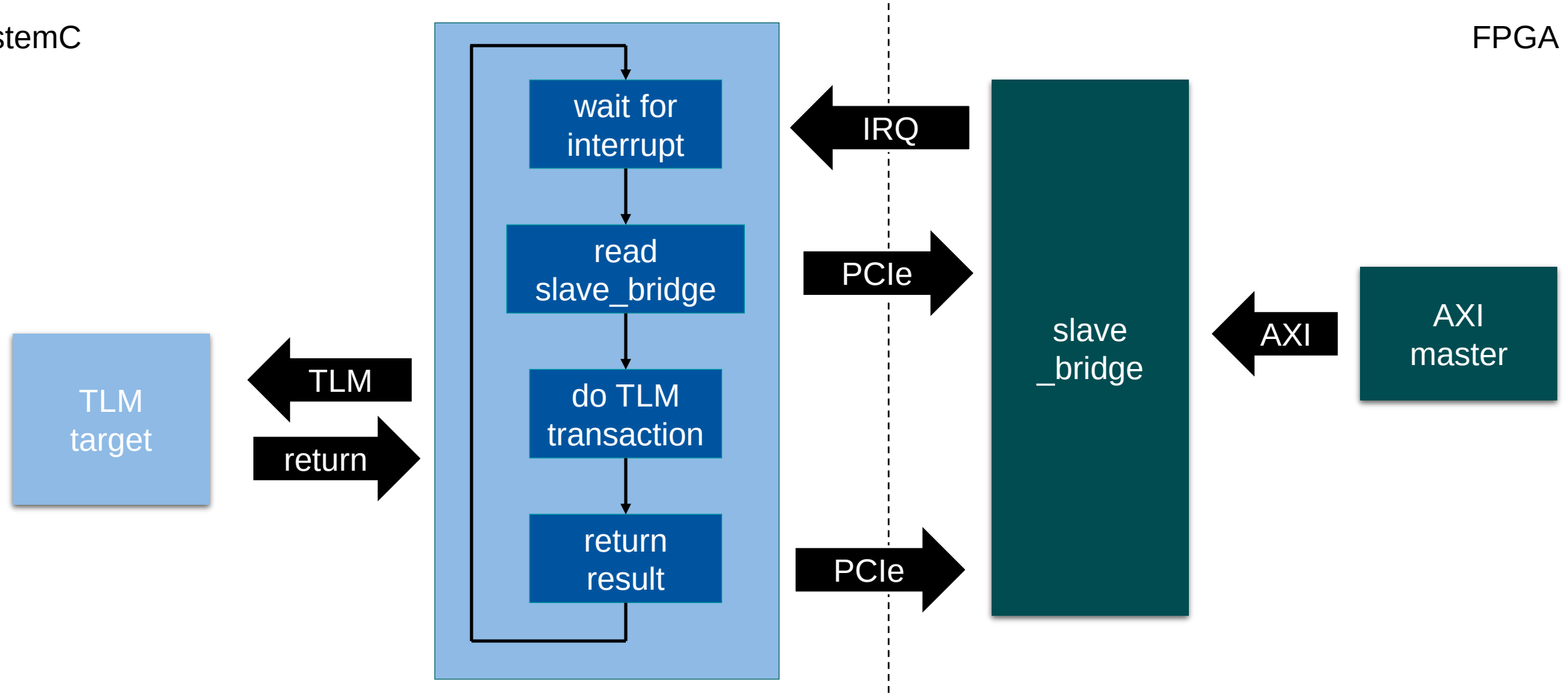
Software Architecture



Dataflow Master Connection



Dataflow Slave Connection



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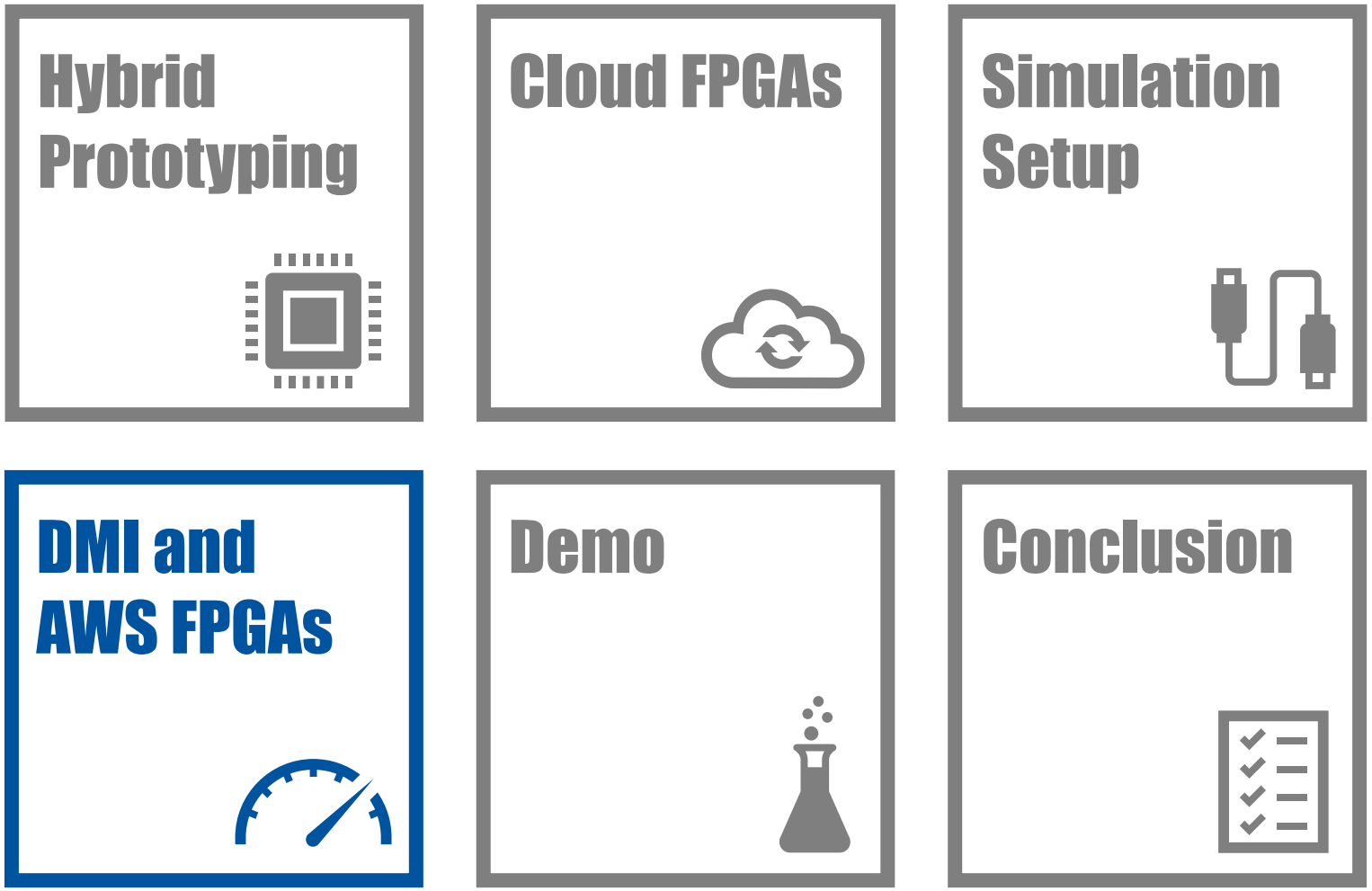
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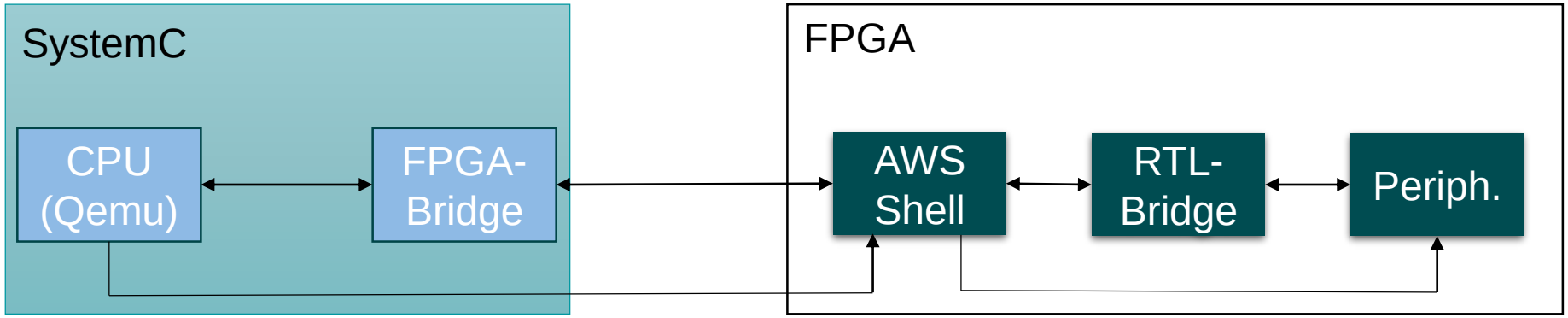
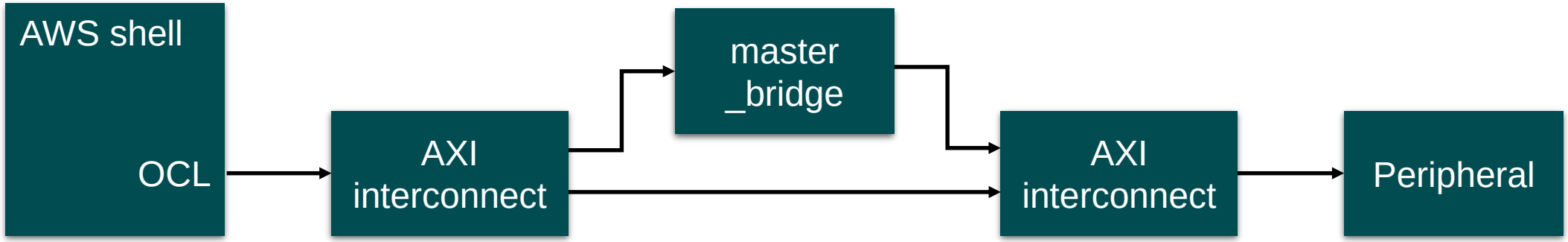
Optimization for SystemC TLM



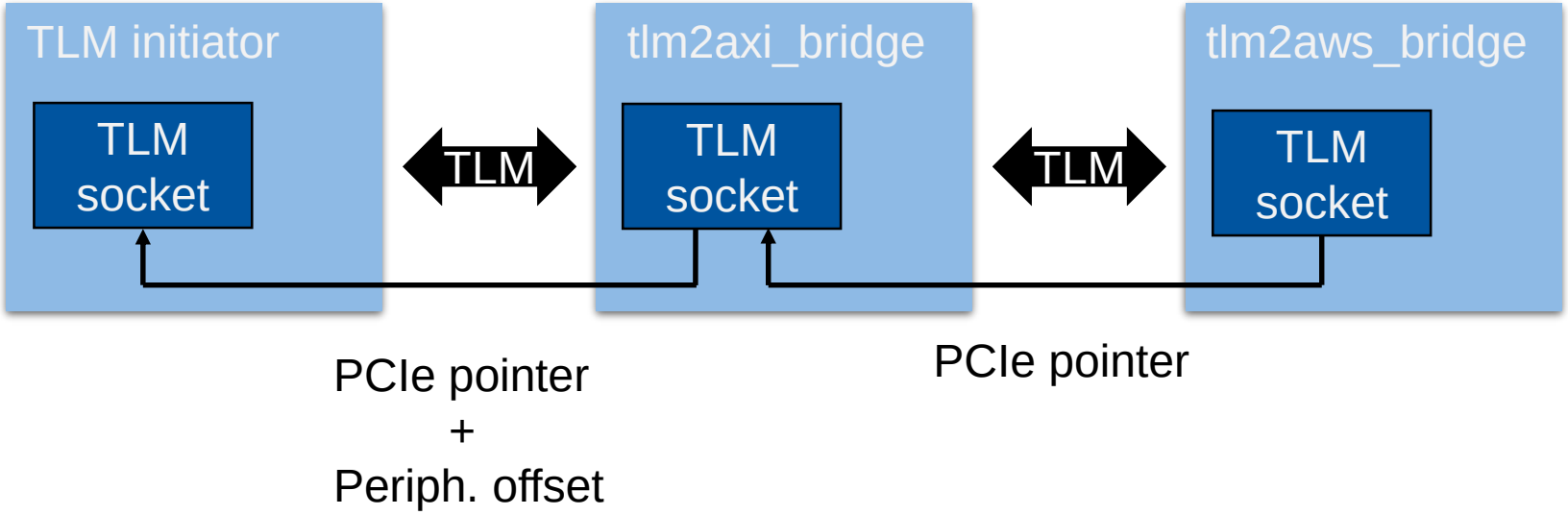
Direct Memory Interface (DMI)

Optimization for SystemC TLM (Hardware)



RTL module	Address range
master_bridge	0x0000_0000 – 0x0020_0000
Peripheral	0x0020_0000 – 0x0200_0000

Optimization for SystemC TLM (Software)



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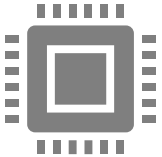
- Hybrid Prototyping 
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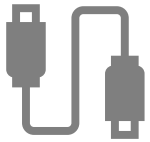
- Simulation Setup 
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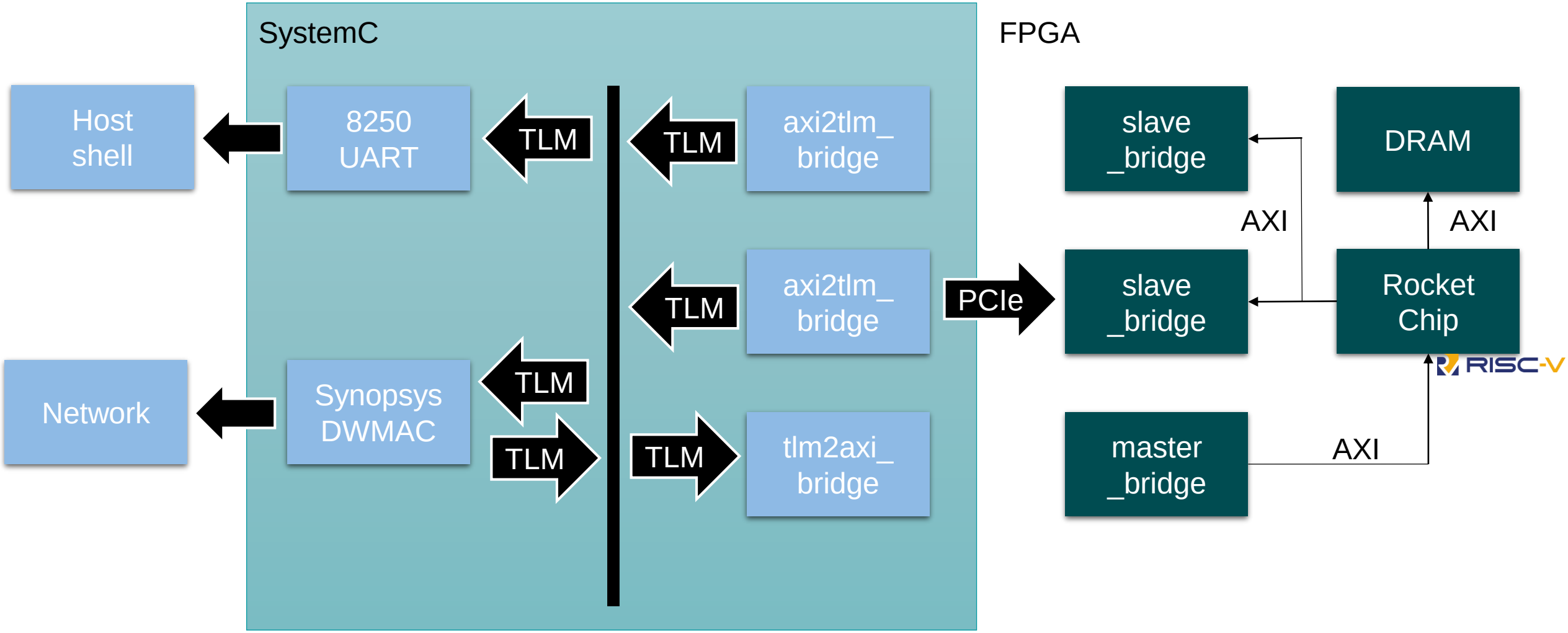
Demo



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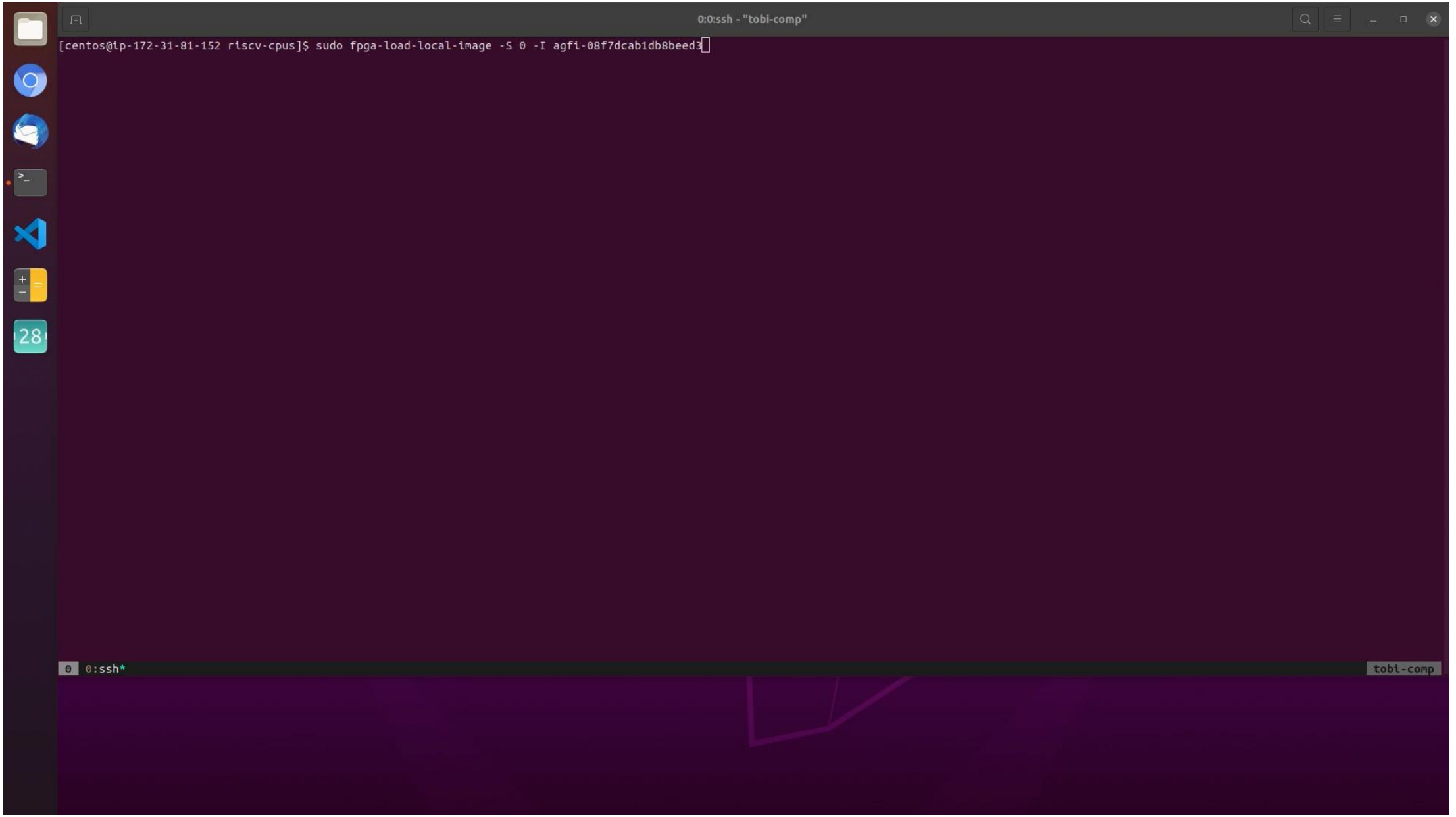

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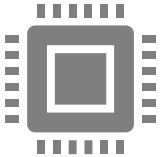
- Hybrid Prototyping 
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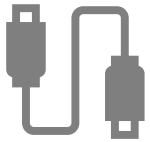
- Simulation Setup 
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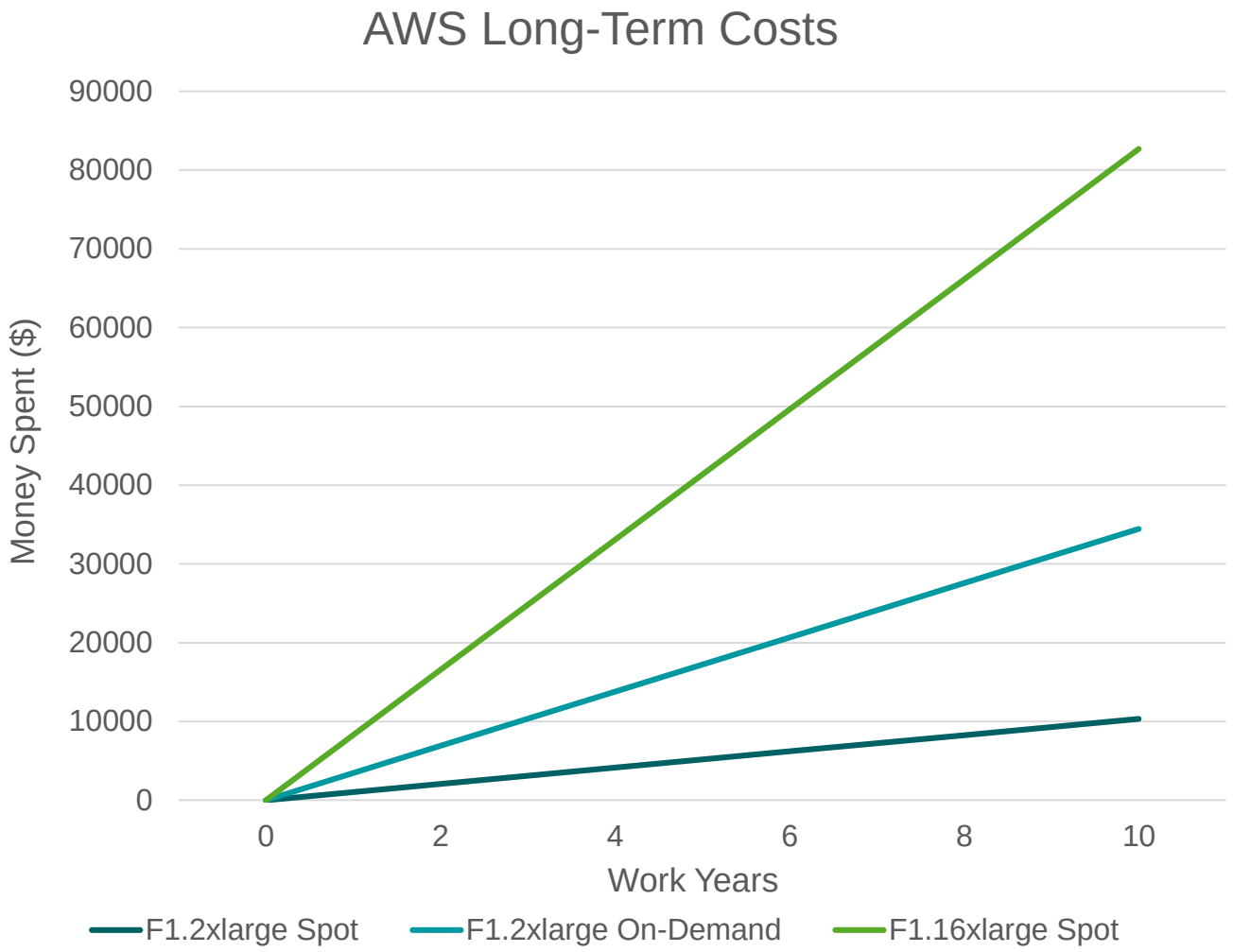
Conclusion

- Cloud-based Hybrid Protoyping offers
  - Low entry barrier, pay as you go
  - Availabilty of latest FPGAs
  - Scaleability
- We demonstrated
  - Hybrid Prototype of RISC-V Linux system
  - Optimization for SystemC DMI usage
- Future Work
  - DMI from FPGA to SystemC
  - Multi-Core
  - Extension to emulation

Thank you!



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